芯海科技
CHIPSEA

CS1238user manual

24-bit Sigma-Delta ADC

Rev 1.1

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Version history

historic version	Modify content	version date
REV 1.0	initial version	2014-3-26
REV 1.1	1.Change format 2.Modify differential input impedance parameters 3.RevisePPNoise parameters 4.Modify common mode input range parameters	2014-10-17

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1Chip function description

CS1238It is a high-precision, low-power analog-to-digital conversion chip with two differential input channels, built-in temperature sensor and High precision oscillator.

CS1238ofPGAOptional:1,2,64,128,The default is128.

CS1238ofADCData output rates are optional:10Hz,40Hz,640Hz,1.28kHz,The default is10Hz;

MCUable to pass2linearSPIinterfaceSCLK,*DRDY*/*DOUT*andCS1238communicate, carry out line configuration, such as channel selection,PGAselection, output rate selection, etc.

1.1Main functional features of the chip

- Built-in crystal oscillator
- Integrated temperature sensor
- bringpower downFunction
- 2WireSPIinterface, the fastest rate is1.1MHz

ADCFeatures:

- twenty fourNo missing bits
- PGAOptional magnification:1,2,64,128
- integrated2aisletwenty fourdifferential input with no missing bits, thePGA=128hourENOBfor20.7bit(working in5V)\20.2 bit(working in3.3V)
- PPnoise:PGA=128,10Hz:150nV;
- INLless than0.0015%
- Output rate optional:10Hz,40Hz,640Hz,1.28kHz
- In-band short function

1.2Chip application scenarios

- industrial process control
- electronic scale
- Liquid/Gas Chemical Analysis
- blood meter
- Smart converter
- portable device

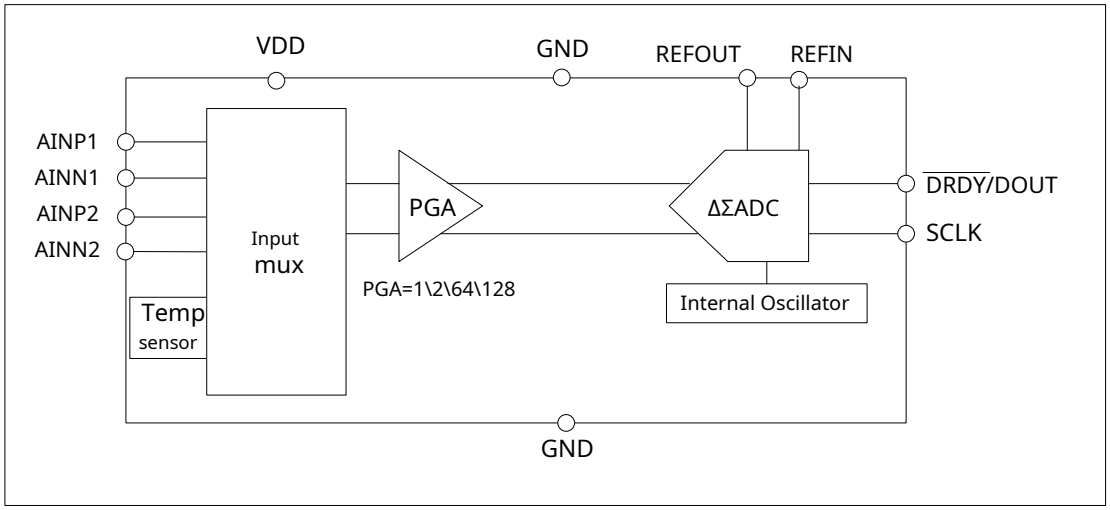
1.3Chip basic structure and function description

CS1238It is a high-precision, low-power consumptionSigma-DeltaAnalog-to-digital conversion chip, built-in oneSigma-Delta ADC, two differential input channels and one temperature sensor,ADCUse two levelssigma deltamodulator, through a low-noise Acoustic instrument is realized with amplifier structurePGAMagnification, optional magnification:1,2,64,128. existPGA=128valid when Resolution up to20.7bit(working in5V).

CS1238built-inRCOscillator, no external crystal required.

CS1238able to pass*DRDY*/*DOUT*andSCLKConfigure multiple functional modes, such as temperature detection,PGAchoose,ADCData output rate selection and more.

CS1238havepower downmodel.



picture1 CS1238Principle block diagram

1.4Chip absolute maximum limit value

surface1 CS1238limit value

name	symbol	smallest	maximum	unit
voltage	VDD	- 0.3	6	V
Power supply instantaneous current			100	mA
Power supply constant current			10	mA
Digital pin input voltage		- 0.3	DVDD+0.3	V
Digital output pin voltage		- 0.3	DVDD+0.3	V
Temperature			150	℃
Operating temperature		- 40	85	℃
Storage temperature		- 60	150	℃
Chip pin soldering temperature			240	℃

1.5 CS1238digital logic properties

surface2 CS1238digital logic properties

parameter	smallest	typical	maximum	unit	Conditions
VIH	0.7×DVDD		DVDD+0.1	V	
VIL	DGND		0.3×DVDD	V	
VOH	DVDD-0.4		DVDD	V	Ioh=1mA
VOL	DGND		0.2×DVDD	V	IoL=1mA
IIH			10	μA	VI=DVDD
IIL	- 10			μA	VI=DGND
Serial clockSCLKworking frequency			1.1	MHz	

1.6 CS1238electrical characteristics

All parameters tested at ambient temperature -40~85℃, built-in reference conditions, unless otherwise noted.

surface3 CS1238Electrical Characteristics (VDD = 5V,3.3V)

parameter	condition	minimum value	typical value	maximum value	unit
Analog input					
Full scale input voltage (AINP-AINN)			±0.5VREF/PGA		V
Common mode input voltage	PGA=1,2	AGND-0.1		AVDD+0.1	V
	PGA=64,128	AGND+0.75		AVDD-0.75	V
Differential input impedance	PGA=1,2		210		MΩ
	PGA=64,128		29		MΩ
system performance					
resolution	No missing codes		twenty four		Bits
ADrate			10	1280	Hz
build time	Fully established	3:ADCThe output rate is10\40Hz, 4: ADCThe output rate is640\1280Hz			conversion cycle
PPnoise	PGA=128,10Hz		150		nv
Effective accuracy	PGA=128,10Hz		20.7(5V) 20.2(3.3V)		bit
Integral linearity	PGA=128		±15		ppm
offset error	PGA=128		±1.4		μV
offset error drift	PGA=128		20		nv/℃
gain error	PGA=128		±0.5		%
Gain error drift	PGA=128		8		ppm/℃
Reference voltage input					
Reference voltage input	REFIN	1.5	VDD	VDD+0.1	V
Reference voltage output					
Reference voltage output	REFOUT		VDD		V
clock					
Internal oscillator frequency			5.2		MHz
Built-in clock temperature drift			250		ppm/℃
Temperature Sensor					
Temperature measurement error	TempError		±3		℃

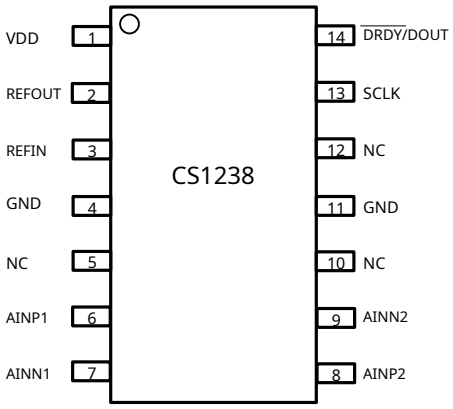
surface4 CS1238Power Supply Electrical Characteristics (VDD = 5V)

parameter	condition		minimum value	typical value	maximum value	unit
voltage	VDD		4.5	5	5.5	V
Working current	normal model	PGA=1,2		1.57		mA
		PGA=64,128		2.34		mA
	power down			0.1	0.1	μA

surface5 CS1238Power Supply Electrical Characteristics (VDD = 3.3V)

parameter	condition		minimum value	typical value	maximum value	unit
voltage	VDD		3	3.3	3.6	V
Working current	normal model	PGA=1,2		1.26		mA
		PGA=64,128		2.11		mA
	power down			0.1		μA

1.7chip pin



picture2 CS1238Chip pin diagram

surface6 PINsFoot description

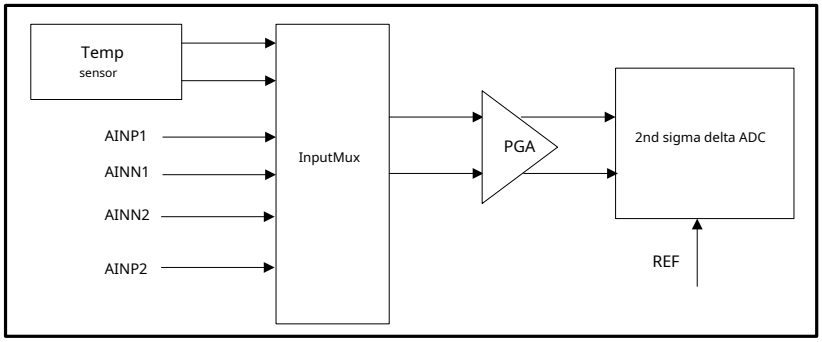
serial number	Pin name	input Output	illustrate
1	VDD	P	power supply
2	REFOUT	AO	Reference source output
3	REFIN	AI	Reference source input
4	GND	P	chip ground
5	NC		Empty feet
6	AINP1	AI	aisle1positive input
7	AINN1	AI	aisle1Negative input
8	AINP2	AI	aisle2positive input
9	AINN2	AI	aisle2Negative input
10	NC		Empty feet
11	GND	P	chip ground
12	NC		Empty feet
13	SCLK	DI	SPIinput interface
14	$\overline{DRDY}$/DOUT	DI/DO	SPIData input/output interface

Note:REFOUTThat is, the sensor excitation source output (the output value isVDD).

2Chip function module description

2.1Analog input front end

CS1238There is1roadADC,Integrated2Channel differential input, the signal input can be a differential input signalAINP1, AINN1orAINP2,AINN2, or it can be the output signal of the temperature sensor. The input signal is switched by the register (ch_sel[1:0])Control, its basic structure is shown in the figure below:



picture3Analog input structure diagram

CS1238ofPGACan be equipped with:1,2,64,128, by the register (pga_sel[1:0])control;

The reference voltage can be externally input or internally output. If you want to use an external reference voltage, you must first turn off the internal reference, the internal reference is controlled by register (refo_off)control.

2.2Temperature Sensor

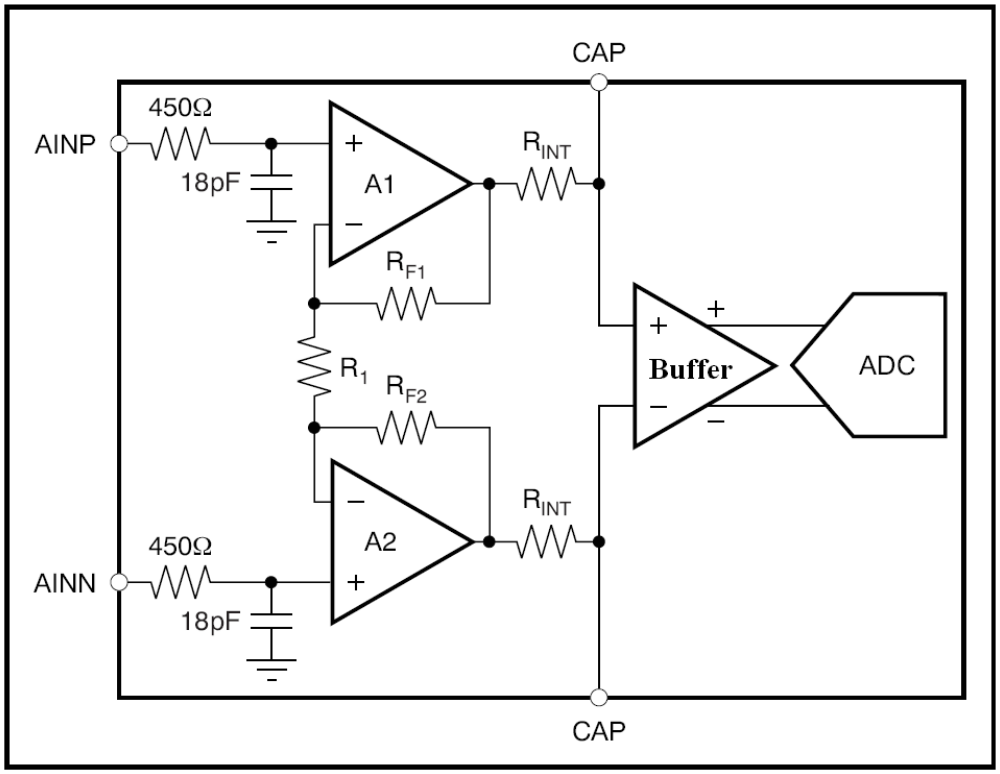
The temperature measurement function is provided inside the chip. whench_sel[1:0]=2'b10hour,ADCThe analog signal input is connected to the internal temperature sensor sensor, other analog input signals are invalid.ADCThe actual actual temperature value. whench_sel[1:0]=2'b10hour,ADCOnly supportsPGA=1.**The temperature sensor needs to be calibrated at a single point just. Correction method: at a certain temperature pointANext, use the temperature sensor to measure and get the code valueYa.**

Then other temperature pointsBCorresponding temperature =Yb*(273.15+A)/Ya-273.15

AThe unit of temperature is degrees Celsius.YayesAThe point corresponds to the temperature code value.YbyesBThe point corresponds to the temperature code value.

2.3low noisePGAamplifier

CS1238provides a low noise, low driftPGAThe amplifier is connected to the bridge sensor differential output, which is based on This structural diagram is shown in the figure below. The front resistorEMIfilter circuitR=450Ω,C=18pFaccomplish20MHigh frequency filtering. Low noisePGAAmplifier passesRF1,R1,RF2accomplish64times amplification, and combined with the switching capacitor of the subsequent stagePGAcomposition64and 128ofPGAenlarge. passpga_sel[1:0]to configure1,2,64,128etc. differentPGA. when using PGA=1,2hour,64times lower noisePGAThe amplifier is shut down to save power. When using low noisePGAamplifier When , the input range is withinGND+0.75VarriveVDD-0.75VBetween, exceeding this range will lead to actual performance degradation. existCAPThe port is connected to a built-in45pFcapacitor, with built-in2kresistanceRINTForm a low-pass filter for low-noise VoicePGAhigh-frequency filtering of the amplifier output signal, while the low-pass filter can also be used asADCanti-aliasing filter device.



picture4 PGAstructure diagram

CS1238built-inBuffer,whenPGA=1,2hour,CS1238useBufferto reduce due toADCDifferential input Problems caused by low impedance, such as insufficient settling time, large gain error, etc., whenPGA=64,128hour, CS1238also useBufferto reduce noise due to lowPGAgo throughRINT=2K,CINT=0.1μFAfter low-pass filtering The phenomena caused by the establishment error, gain error and internal code drift.

2.4clock signal source

CS1238Use the built-in crystal oscillator to provide the clock frequency required by the system. The typical value is5.2MHz.

2.5Reset and power down (POR&power down)

When the chip is powered on, the built-in power-on reset circuit will generate a reset signal to automatically reset the chip.

whenSCLKgoes from low to high and remains high for more than100μs,CS1238EnterPowerDwon mode, when the power consumption is lower than0.1μA. whenSCLKWhen returning to low level, the chip will re-enter normal working state. state.

When the system consists ofpower downWhen re-entering normal working mode, all functions are configured asPowerDownOf In the current state, no function configuration is required.

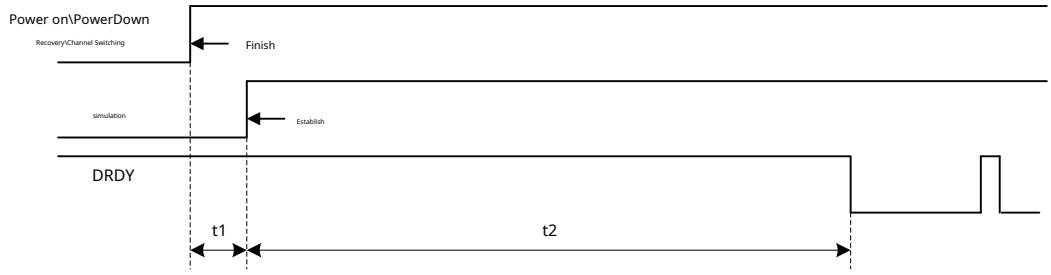
2.6 SPISerial communication

CS1238adopted in2WireSPIserial communication viaSCLKand*DRDY*/*DOUT*It can realize data reception and function configuration.

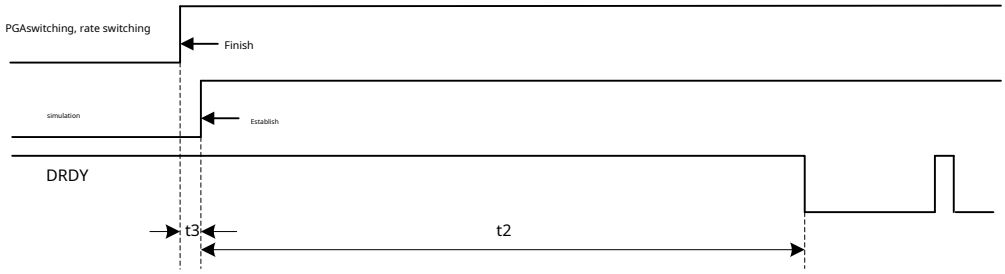
2.6.1 build time

existADCThe data output rate is10Hzor40HzWhen , the digital part needs to have3data conversion cycle satisfies the modulus The establishment of the intended input signal and the establishment time requirements of the filter;ADCThe data output rate is640Hzor1280Hzhour, The digital part needs to be4The data conversion cycle meets the settling time requirements of the analog input signal and the filter.

CS1238The entire establishment process is shown in the figure below:



picture5 CS1238Data creation process1



picture6 CS1238Data creation process2

parameter	describe(1)		minimum value	typical value	maximum value	unit
t1	Power on\PowerDownSetup time required for simulation after recovery\channel switch			2		ms
t3	PGASetup time required for simulation after switching\rate switching			0.8		μs
t2	Creation time (*DRDY*/*DOUT*Keep power high flat)	10\40Hz		300\75		ms
		640\1280Hz		6.25\3.125		ms

2.6.2 ADCData output rate

CS1238The data output rate can be set by registerspeed_sel[1:0]configuration.

surface7Output rate setting

SPEED_SEL[1:0]	ADCoutput rate (Hz)
00	10
01	40
10	640
11	1280

2.6.3 Data Format

CS1238The output data istwenty fourbit2Hexadecimal complement, MSB (MSB) is output first. least significant digit (LSB)for$(0.5V_{REF}/Gain)/(2_{twenty\ three}-1)$. A positive full-scale output code is7FFFFFH, the negative value full-scale output code is 800000H. The following table shows the ideal output codes corresponding to different analog input signals.

surface8Ideal output code and input signal(1)

input signalV_{IN}(AINP-AINN)	ideal output
≥$+0.5V_{REF}/Gain$	7FFFFFH
$(+0.5V_{REF}/Gain)/(2_{twenty\ three}-1)$	000001H
0	000000H
$(-0.5V_{REF}/Gain)/(2_{twenty\ three}-1)$	FFFFFFH
≤$+0.5V_{REF}/Gain$	800000H

(1) does not consider noise,INL, the effects of offset error and gain error

2.6.4 Data preparation/data input and output ($\overline{DRDY/DOUT}$)

$\overline{DRDY/DOUT}$The pins are4purpose. First, when the output is low, it means that the new data has been converted; Second, as a data output pin, when the data is ready, the1indivualSCLKAfter the rising edge of$\overline{DRDY/DOUT}$ Output the highest bit of the converted data (MSB). in everySCLKon the rising edge, the data will automatically shift1Bit. existtwenty fourindivual SCLKLater alltwenty fourbit data readout, if this time pausesSCLKof sending,$\overline{DRDY/DOUT}$will remain holds the last bit of data until the next data is ready, and then pulls it high.$\overline{DRDY/DOUT}$was pulled again Low, indicating that the new data has been converted and the next data can be read; third, in the25,26indivualSCLK When, the register status update flag is output; fourth, as a register data writing or reading pin, when the register needs to be configured or when reading a register value,SPINeed to send46indivualSCLK,according to$\overline{DRDY/DOUT}$The input command word is judged Determine whether the operation is to write a register or to read a register.

2.6.5 Serial clock input (SCLK)

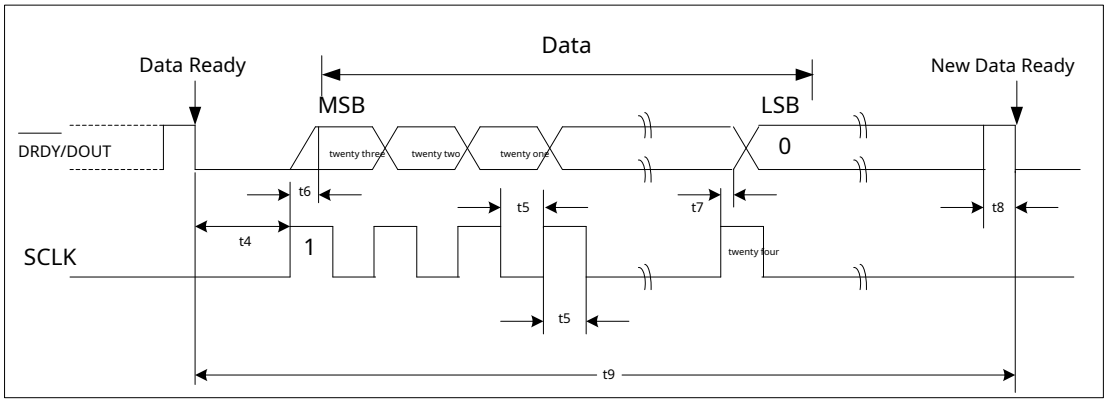
serial clock inputSCLKis a digital pin. This signal should be guaranteed to be a clean signal, glitchy or slow A rising edge may cause incorrect data to be read or an error state to be entered. Therefore, it should be ensuredSCLKof rising and falling are less than50ns.

2.6.6 Data sending

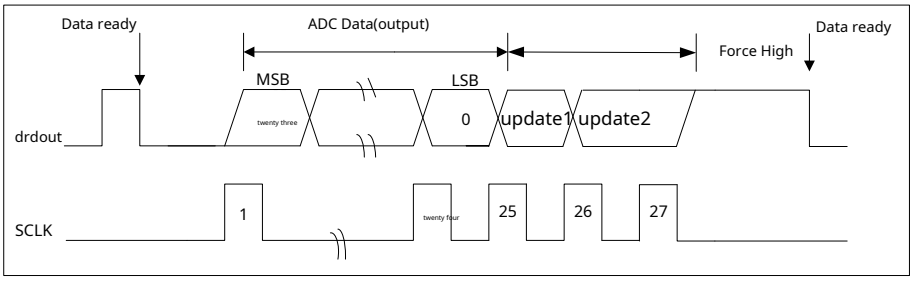
CS1238can continuously convert analog input signals, when the*DRDY/DOUT*pulled low, indicating that the data has been ready to accept, the first to enterSCLKto read the most significant bit of the output, thetwenty fourindivualSCLKwill all later oftwenty fourbit data readout, if this time pausesSCLKof sending,*DRDY/DOUT*will keep the last digit

According to, until it is pulled high, the25and26indivualSCLKWhether the output configuration register has a write operation flag, Section25indivual SCLKcorresponding*DRDY/DOUT*for1When indicating the configuration registerConfigis written with new values, the26indivual SCLKcorresponding*DRDY/DOUT*Reserved for chip expansion, the current output has always been0, through the27indivualSCLK can*DRDY/DOUT*Pull it up, and then be*DRDY/DOUT*is pulled low again, indicating that new data is ready

Get ready to accept and proceed to the next data conversion. Its basic timing is shown in the figure:



picture7 CS1238Read data timing diagram1



picture8 CS1238Read data timing diagram2

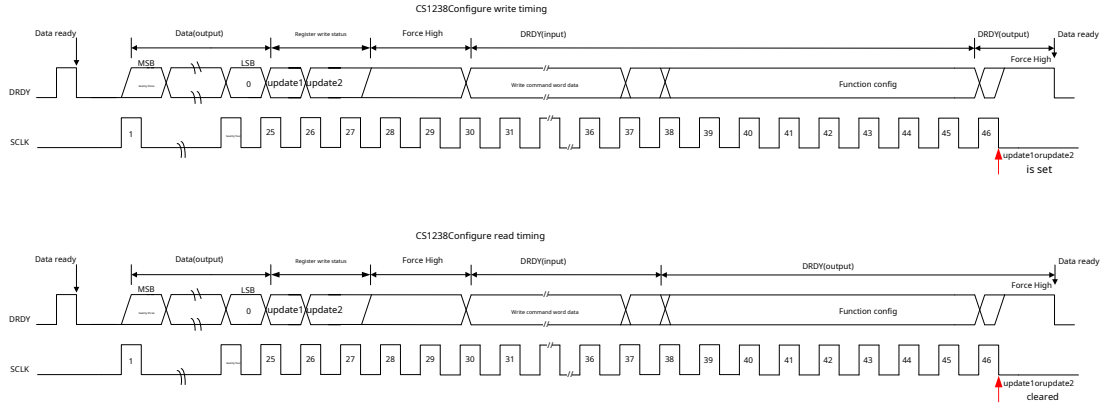
surface9Read data timing table

SYMBOL	DESCRIPTION		MIN	TYP	MAX	UNITS
t4	*DRDY/DOUT*after going low to the firstSCLKrising edge		0			ns
t5	SCLKHigh level or low level pulse width		455			ns
t6	SCLKRising edge to new data bit valid (transmission delay)		455			ns
t7	SCLKRising edge to old data bit valid (hold time)		227.5		455	ns
t8	Data update, reading previous data is not allowed			26.13		μs
t9	conversion time (1/data rate)	10Hz		100		ms
		40Hz		25		ms
		640Hz		1.5625		ms
		1280Hz		0.78125		ms

2.6.7 Function configuration

CS1238able to pass SCLK and $\overline{DRDY/DOUT}$ Different functions can be configured and the function configuration timing sequence

The picture is shown below:



picture9Function configuration timing diagram

A brief description of the function configuration process is given in $\overline{DRDY/DOUT}$ after changing from high to low:

1.No.1to the firsttwenty fourindivualSCLK, readADCdata. If there is no need to configure the register or read the register register, you can omit the following steps.

2.No.25to the first26indivualSCLK, read the register write operation status.

3.No.27indivualSCLK,Bundle $\overline{DRDY/DOUT}$ The output is pulled high.

4.No.28to the first29indivualSCLK, switch $\overline{DRDY/DOUT}$ for input.

5.No.30to the first36indivualSCLK, input register to write or read command word data (high bit input first).

6.No.37indivualSCLK, switch $\overline{DRDY/DOUT}$ direction (if writing a register, $\overline{DRDY/DOUT}$ is input; if it is to read a register, $\overline{DRDY/DOUT}$ for output).

7.No.38to the first45indivualSCLK, input register configuration data or output register configuration data (high bit first input/ output).

8.No.46indivualSCLK, switch $\overline{DRDY/DOUT}$ for output and put $\overline{DRDY/DOUT}$ Pull high. update1/ update2is set or cleared.

2.6.7.1 SPICommand word

CS1238have2command words, the length of the command word is7bits, the command words are described as follows:

surface10 CS1238Command word description table

command name	command byte	describe
Write configuration register	0x65	Write configuration registerConfig
Read configuration register	0x56	Read configuration registerConfig

2.6.7.2 SPIregister

CS1238There is a set of registersConfig.

Configregister

register	R/W	describe	reset value
describe	Reserved bit	configuration register	0x0C

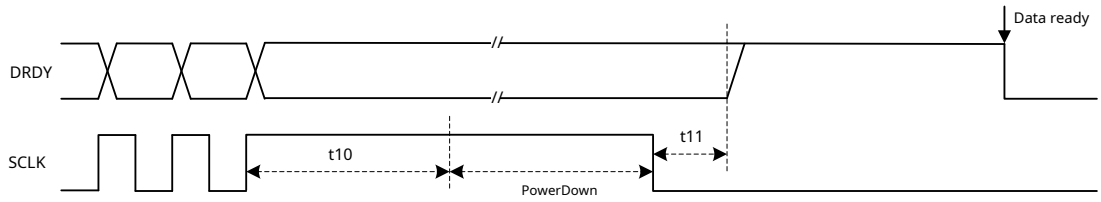
Configuration bits	B7	B6	B5	B4
describe	Reserved bit	REFOutput switch	ADCOutput rate selection	
Configuration bits	B3	B2	B1	B0
describe	PGAchoose		channel selection	

surface11 ConfigRegister description table

Bits	describe	
[7]	-	The chip reserves usage bits.**The default is0, write when writing0, don't write1**
[6]	REFO_OFF	**REFOutput switch:**defaultREFoutput on 1=closureREFoutput. 0=REFNormal output.
[5:4]	SPEED_SEL	**ADCOutput rate selection:**The default is10Hz SPEED_SEL[1:0] / describe 00 / ADCThe output rate is10Hz 01 / ADCThe output rate is40Hz 10 / ADCThe output rate is640Hz 11 / ADCThe output rate is1280Hz
[3:2]	PGA_SEL	**PGAchoose:**defaultPGAfor128, in temperature measurement modePGA_SEL=00 PGA_SEL[1:0] / describe 00 / 1 01 / 2 10 / 64 11 / 128
[1:0]	CH_SEL[1:0]	**channel selection**: The default channel is channelA CH_SEL[1:0] / describe 00 / aisleA 01 / aisleB 10 / temperature 11 / short inside

2.6.8 Power downmodel

whenSCLKgoes from low to high and remains high for more than100μs,CS1238EnterPowerDwon mode, all circuits of the chip will be turned off at this time, and the power consumption is close to0. whenSCLKWhen returning to low level, the chip will re-enter normal working state.



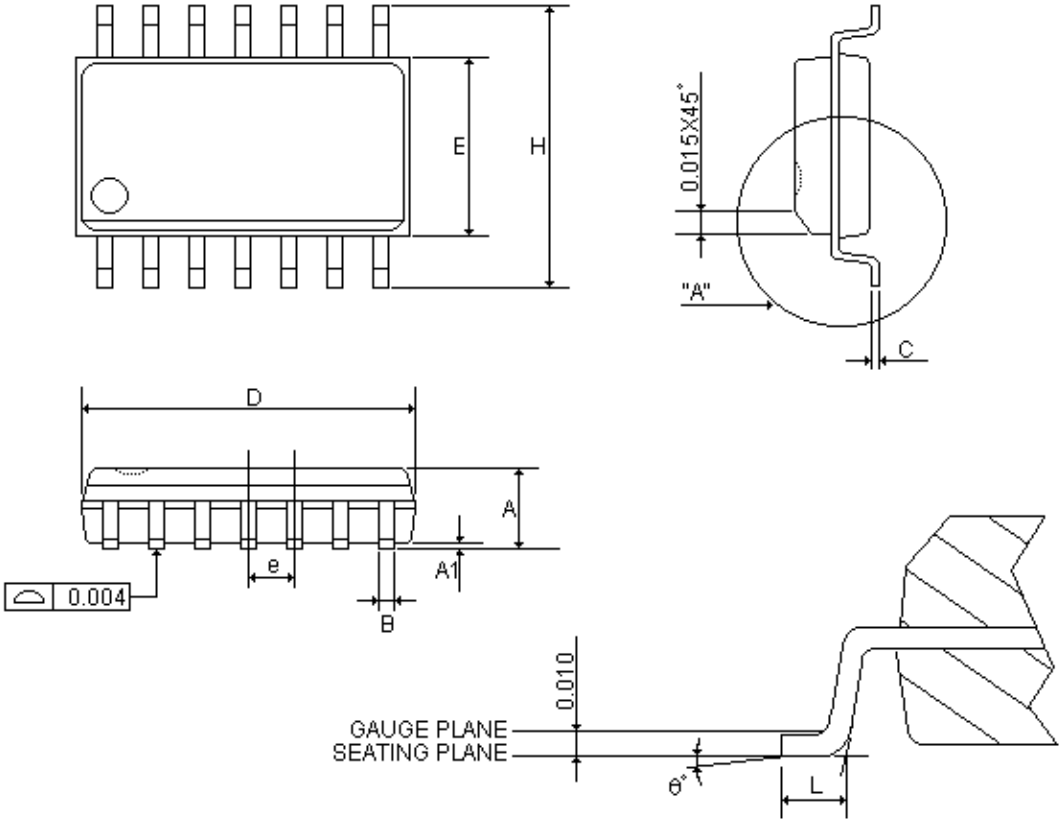
picture10 CS1238 PowerDownSchematic diagram of the model

symbol	describe	minimum value	typical value	maximum value
t10	SCLKHigh level hold time	100μs		
t11	SCLKLow level hold time after falling	10μs		

3Chip packaging

CS1238useSOP14\DIP14Encapsulation.

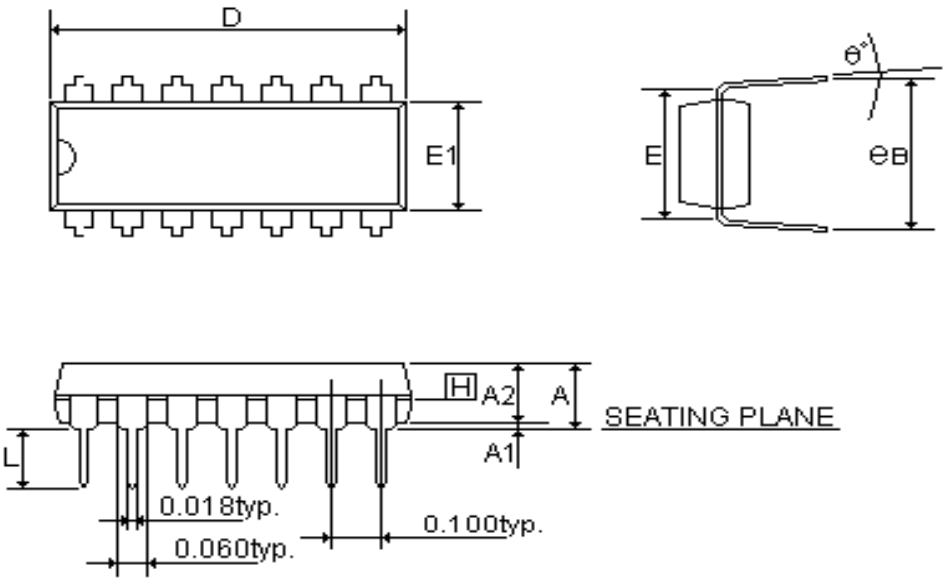
3.1 SOP-14pin



picture11chipSOP14Package size information

SYMBOLS	MIN	NOR	MAX
	(mm)		
A	1.473	1.625	1.727
A1	0.101	-	0.254
B	0.330	0.406	0.508
C	0.190	0.203	0.249
D	8.534	8.661	8.737
E	3.810	3.911	3.987
e	-	1.270	-
H	5.791	5.994	6.197
L	0.381	0.635	1.270
θ°	0°	-	8°

3.2 DIP-14pin



picture12chipDIP14Package size information

SYMBOLS	MIN	NOR	MAX
	(mm)		
A	-	-	5.334
A1	0.381	-	-
A2	3.175	3.302	3.429
D	18.669	1.905	19.685
E		7.62	
E1	6.223	6.35	6.477
L	2.921	3.302	3.810
eB	8.509	9.017	9.525
θ°	0°	7°	15°